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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,209	09/12/2000	Charles W. Mitchell	1001-0135	6900

22120 7590 05/05/2005

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EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/660,209	MITCHELL ET AL.	
	Examiner	Art Unit	
	Tung S. Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13,15,18,20-23,26-29,34 and 36-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-13,15,18,20-23,26-29,34 and 36-39* is/are rejected.

7)☒ Claim(s) *6 and 40-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 13, 20, 23, 27, 38, 3, 4, 5, 7, 8, 9, 10, 11, 12, 15, 18, 21, 22, 26, 28, 29, 34, 36, 37, 39 are rejected under 35 U.S.C. 102(e) as being anticipated Hussain et al. (U.S. patent 6,172,611).

Regarding claim 1:

Hussain discloses an integrated circuit comprising a temperature sensor providing a temperature measurement of the integrated circuit (Col. 1-2, Lines 57-9); a programmable storage location storing a first temperature limit value (Col. 2-3, Lines 40-16), the programmable storage location accessible via an instruction executed by the integrated circuit (Col. 2-3, Lines 40-16); and compare logic coupled to the temperature sensor and the storage location to provide an indication of a comparison between the temperature measurement and the first temperature limit value (Col. 2-3, Lines 40-16), wherein the integrated circuit asserts a first temperature control signal which is supplied on a

first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value (Col. 2-3, Lines 40-16).

Regarding claim 13:

Hussain discloses a method comprising measuring a temperature of an integrated circuit with a temperature sensor (Col. 1-2, Lines 57-9), the temperature sensor being a circuit within the integrated circuit (Col. 1-2, Lines 57-9); comparing the measured temperature to a first limit value stored in the integrated circuit (Col. 2-3, Lines 40-16); and generating a signal on a first output terminal of the integrated circuit according to the comparison to control the temperature of the integrated circuit (Col. 2-3, Lines 40-16), wherein the signal is asserted when the measured temperature is greater than the first limit value (Col. 2-3, Lines 40-16), and wherein the signal on the first output terminal is deasserted according to a programmable mode of operation that included deasserting in response at least one to a control location on the integrated circuit is being accessed andr the measured temperature falling below a lower limit value (Col. 2-3, Lines 40-16).

Regarding claim 20:

Hussain discloses a method including measuring a temperature of an integrated circuit with a temperature sensor (Col. 1-2, Lines 57-9), the temperature sensor being a circuit within the integrated circuit (Col. 1-2, Lines 57-9); comparing the measured temperature to a first limit value stored in the integrated circuit;

generating a signal on a first output terminal of the integrated circuit according to the comparison to control the temperature of the integrated circuit (Col. 2-3, Lines 40-16); and accessing a control location in the integrated circuit to cause the signal to be deasserted (Col. 2-3, Lines 40-16, fig. 3, unit 360).

Regarding claim 23:

Hussain discloses a method comprising measuring a temperature of an integrated circuit with a temperature sensor (Col. 1-2, Lines 57-9), the temperature sensor being a circuit within the integrated circuit (Col. 1-2, Lines 57-9); comparing the measured temperature to a first limit value stored in the integrated circuit (Col. 2-3, Lines 40-16, fig. 3, unit 350); and generating a signal on a first output terminal of the integrated circuit according to the comparison to control the temperature of the integrated circuit (Col. 2-3, Lines 40-16, fig. 3, unit 360); comparing the measured temperature to a second limit value stored in the integrated circuit; and asserting a second signal on a second output terminal of the integrated circuit when the measured temperature is above the second limit value, thereby indicating that the temperature has exceeded a safe limit (Col. 2-3, Lines 40-16, fig. 3, unit 360) and deasseting the second signal by accessing a control location in the integrated circuit (fig. 2, unit 222, 224, 230, 232, 242) .

Regarding claim 27:

Hussain discloses a microprocessor comprising a temperature sensor providing a temperature measurement of the integrated circuit (Col. 1-2, Lines 57-9); at

least a first and second temperature limit value stored in programmable storage locations in the microprocessor (Col. 2-3, Lines 40-16, fig. 3, unit 315, fig. 1, unit 130), the storage locations being accessible via software executed by the microprocessor (fig. 2, unit 230); compare logic coupled to the temperature sensor and to the programmable storage locations storing the first and second temperature limit values (Col. 2-3, Lines 40-16), to provide respectively a first and second signal indicative of a comparison between the temperature measurement and the first and second temperature limit values; and first and second output terminals coupled to provide respectively, the first and second signals (Col. 2-3, Lines 40-16, fig. 3, unit 350, 360).

Regarding claim 38:

Hussain discloses an apparatus comprising: a processor that includes control registers operable to host temperature limit values, mean for comparing a temperature to at least a first and second of the limit values, means for providing a control signal on a first output terminal of the processor according to the comparison of the measured temperature to the first limit value, the control signal to control the temperature of the integrate circuit, means for providing an indicator on a second output terminal of the integrated circuit when the measured temperature is above the second limit value, thereby indicating that the measured temperature has exceeded a safe limit; and means for making the

control registers accessible to software that monitors temperatures ans sets a thermal management mode for the apparatus.

Regarding claims 3, 4, 5, 7, 8, 9, 10, 11, 12, 15, 18, 21, 22, 26, 28, 29, 34, 36, 37, 39:

Hussain continues to disclose temperature is above limit, below the temperature range (Col. 2-3, Lines 40-16), deasserts the signals in response to temperature changes according to mode of operation (Col. 2-3, Lines 40-16, fig. 3, unit 355, 365), storage location is addressable accessible by instruction (fig. 4, unit 430, 440, 450, fig. 3, unit 320, 350, 360), temperature comparison is external to the IC to asset signal (fig. 4, unit 432), contains second storage unit (fig. 2, unit 230), third storage unit (fig. 2, unit 240)), below to a third limit value (fig. 3, unit 360)), the IC is microprocessor (Col. 1, Lines 5-10, fig. 1, unit 130), the signal is used to inhibit cooling device to control temperature (fig. 1, unit 152), direct control a cooling device (fig. 1, unit 160), use sequence of instruction cause the signal to be deasserted (fig. 3, unit 320, 350, 360), a control location in the IC, including at least one cooling device in response to asserted signal (fig. 3, unit 320), software accessable control register (fig. 4, unit 430), indication of the compare logic (fig. 3, unit 320, 350, 360), control temperature when excess the reference temperature (Col. 2-3, Lines 40-16, fig. 4, unit 436, 438, 435, 437, 439), compares to multiple temperatures (fig. 4, unit 431, 432, 435, 436, 437, 438, 439); mapping control register to input output space (fig. 4, 440);

Claim Objections

2. Claims 6, 40, 41 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitation of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: prior art fail to teach the temperature limit value is a panic value, BIOS includes the instruction, BIOS executable to set address for the compare map storage location as input/output space; instruction to assign privilege level to access programmable location.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3. Applicant's arguments filed 4/22/2005 have been fully considered but they are not persuasive.

A. Applicant argues in the arguments that the prior art does not show the 'provides accessibility to a programmable storage location'. Hussain clearly discloses 'provides accessibility to a programmable storage location' in Col. 2-3, Lines 40-16, Col. 6, Lines 20-31, where in fig. 2, register 232-235 in block 230 is the 'provides accessibility to a programmable storage location'.

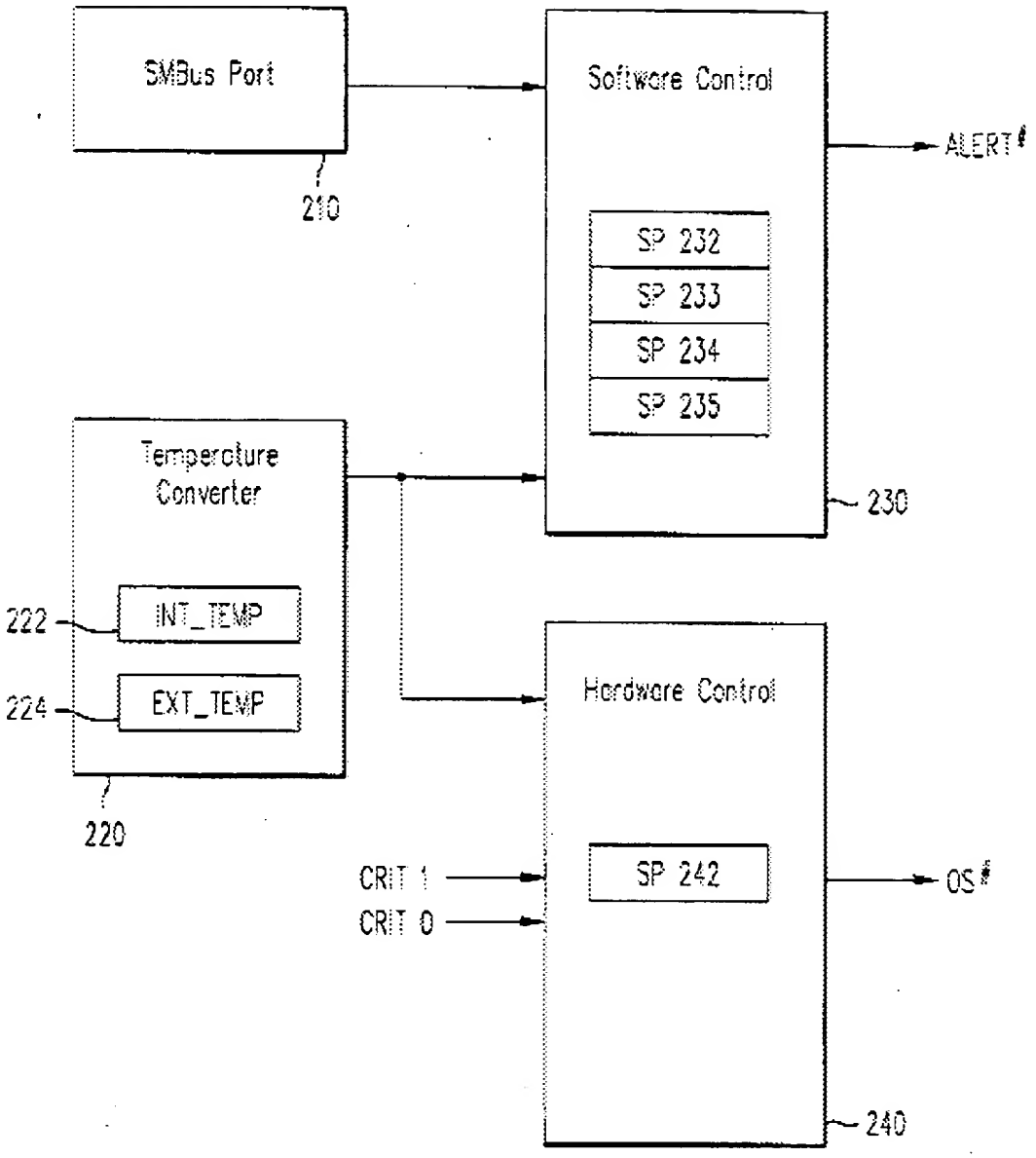

FIG. 2

B. Applicant continues to argue in the arguments that the prior art does not show the 'the signal on the first output terminal is deasserted according to a programmable mode of operation that includes deasaerting in response to at least one of a control location on the integrated circuit being accessed and the

measured'. . Hussain discloses 'the signal on the first output terminal is deasserted according to a programmable mode of operation that includes deasaerting in response to at least one of a control location on the integrated circuit being accessed and the measured' in Col. 2-3, Lines 40-16 and fig. 3, unit 365, fig. 4, unit 440, fig. 5.

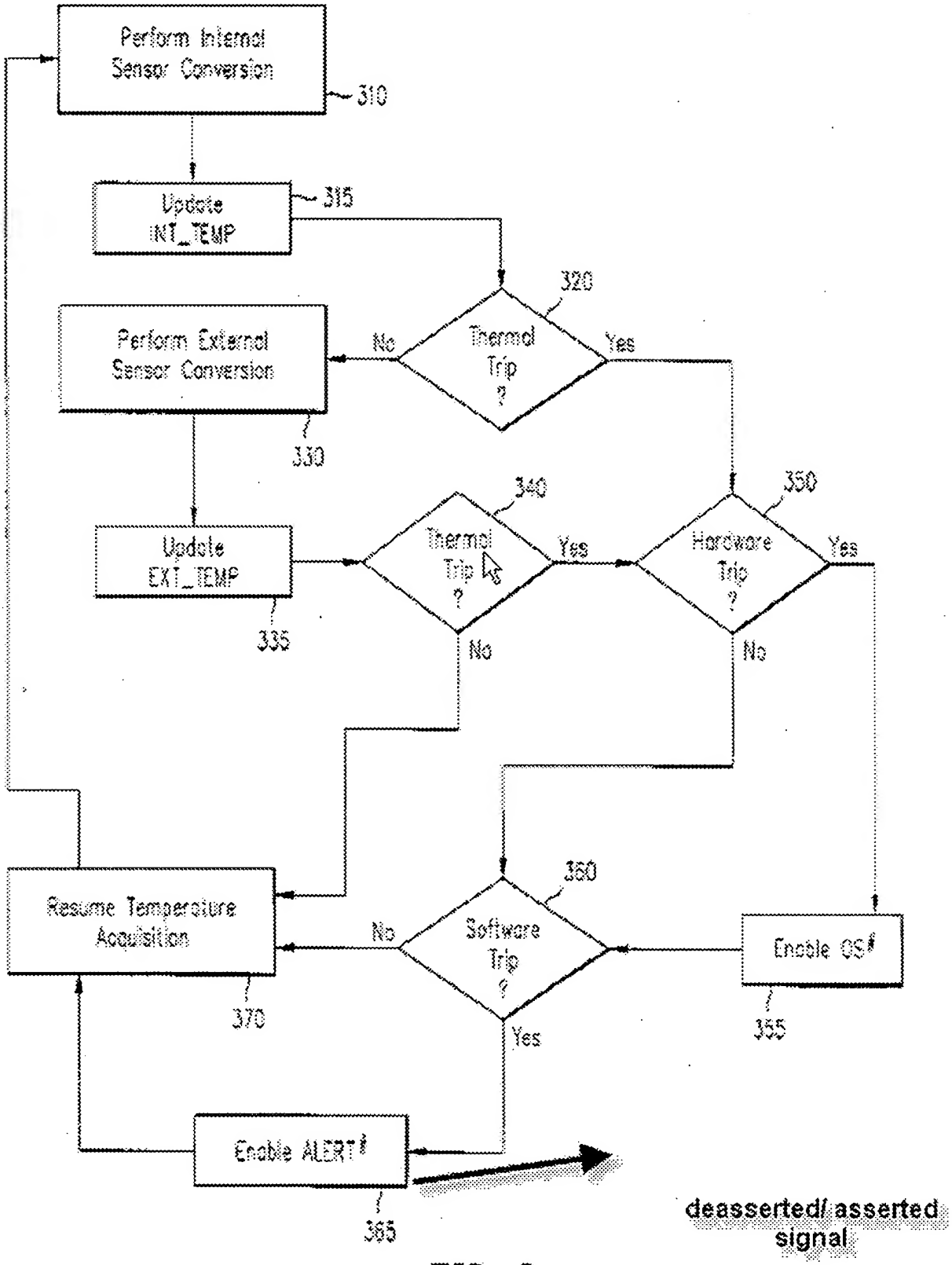
Perform Internal Sensor Conversion
310
Update INT_TEMP
315
320
Thermal Trip ?
No
Yes
Perform External Sensor Conversion
330
Update EXT_TEMP
335
340
Thermal Trip ?
Yes
No
350
Hardware Trip ?
Yes
No
Resume Temperature Acquisition
370
360
Software Trip ?
No
Yes
Enable OS#
355
Enable ALERT#
365
deasserted/ asserted signal

FIG. 3

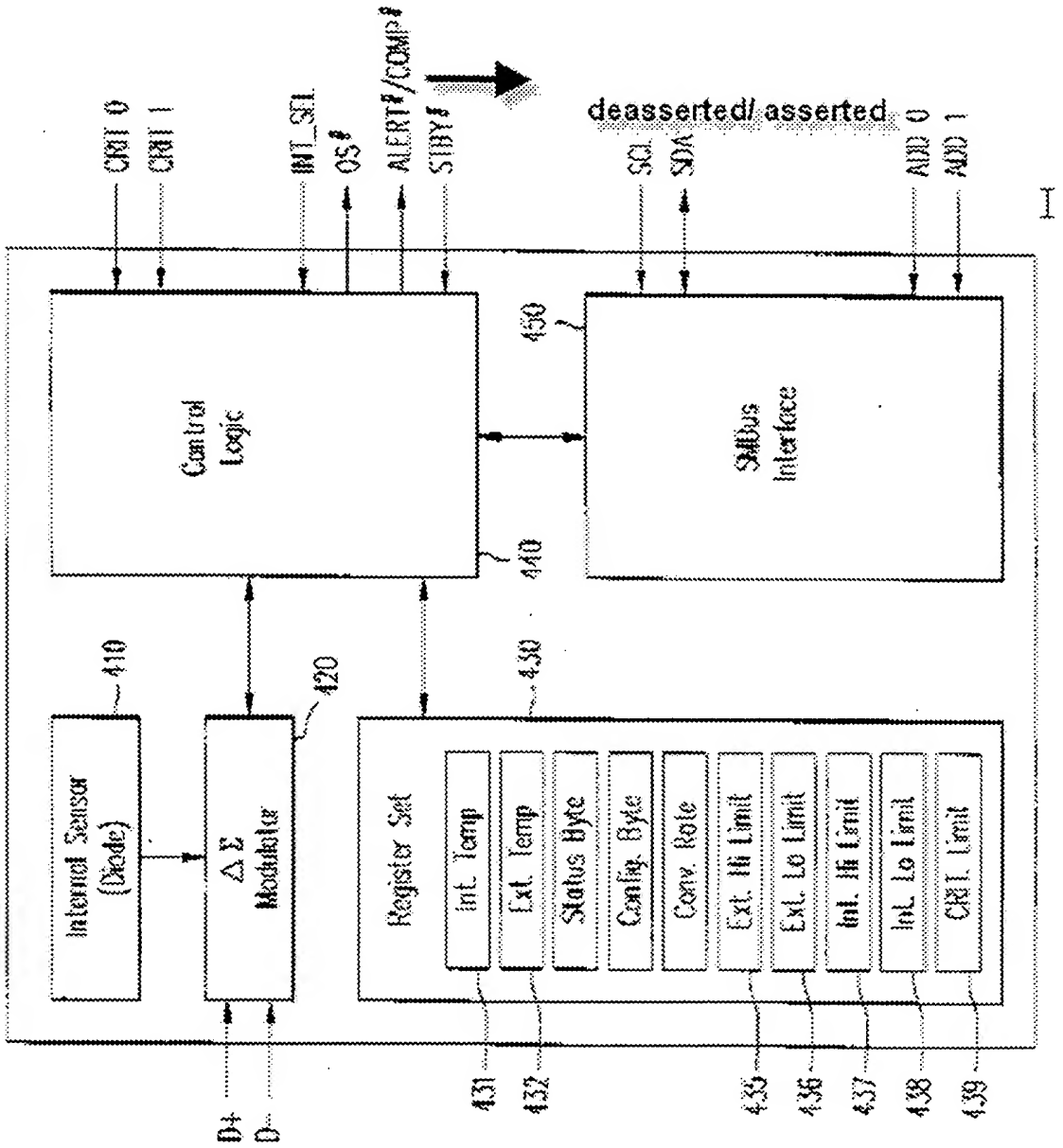
ADD 0
ADD 1
SCL
SDA
deasserted/ asserted
ALERT#/COMP#
STBY#
INT_SEL
OS#
CNFI 0
CNFI 1
SMBus Interface
Control Logic
450
440
410
420
430
Internal Sensor (Diode)
ΔΣ Modulator
Register Set
Int. Temp
Ext. Temp
Status Byte
Config. Byte
Conv. Rate
Ext. Hi Limit
Ext. Lo Limit
Int. Hi Limit
Int. Lo Limit
CNFI. Limit
D+
D-
431
432
435
436
437
438
439

FIG. 4

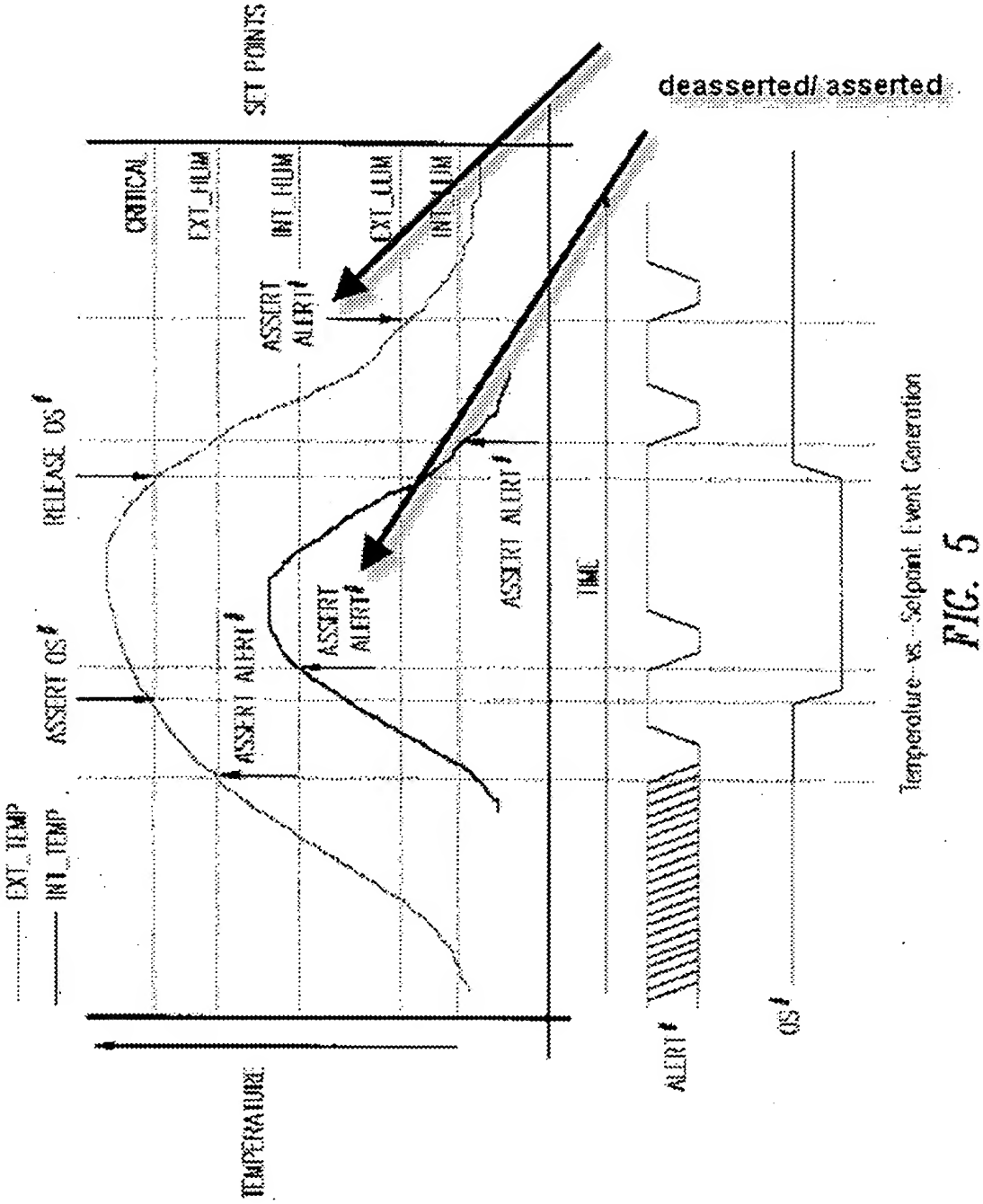

FIG. 5

The examiner reminds to the applicants that during patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification." Applicant always has the opportunity to amend the claims

during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969). While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allowed. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 703-305-3309. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956. TC2800 FAX Telephone Numbers: 703-872-9306

TC2800 Customer Service FAX - (703) 872-9317

TL

John Barlow
Supervisory Patent Examiner
Technology Center 2800